

## **IN THE CLAIMS:**

1. (Amended) A dual mode built-in self-test controller,  
comprising:  
a logic built-in self-test domain, including:  
a logic built-in self-test engine capable of executing a logic built-in self-test; and  
a logic built-in self-test signature generated by an execution of the logic ~~builtin~~  
built-in self-test; and  
a memory built-in self-test domain, including:  
a memory built-in self-test engine capable of executing a memory built-in  
~~selftest~~ self-test;  
wherein the dual-mode built-in self-test controller is geographically centralized  
within an integrated circuit.
2. (Amended) The dual mode built-in self-test controller of claim 1, wherein the  
logic ~~builtin~~ built-in self-test engine comprises:  
a logic built-in self-test state machine; and  
a pattern generator capable of generating a scan pattern for use in a state of the  
logic built-in self-test state machine.
3. (Amended) The dual mode built-in self-test controller of claim 2, wherein the  
logic ~~builtin~~ built-in self-test state machine further comprises:  
a reset state entered upon receipt of an external reset signal;  
an initiate state entered from the reset state upon receipt of a logic built-in self-test  
run signal;  
a scan state entered from the initiate state upon the initialization of components  
and signals in the logic built-in self-test domain in the initiate state;  
a step state entered into from the scan state and from which the scan state is  
entered unless the content of the pattern generator equals a predetermined  
vector count; and

a done state entered into from the step state when the content of the pattern generator equals the predetermined vector count.

4. (Original) The dual mode built-in self-test controller of claim 2, wherein the pattern generator comprises a linear feedback shift register seeded with a primitive polynomial.
5. (Amended) The dual mode built-in self-test controller of claim 2, wherein the logic ~~builtin~~ built-in self-test signature includes at least one of  
a bit indicating an error condition arose; and  
a bit indicating whether the stored results are from a previous logic built-in self-test run.
6. (Original) The dual mode built-in self-test controller of claim 1, wherein the memory built-in self-test domain further comprises a memory built-in self-test signature generated by an execution of the memory built-in self-test.
7. (Cancelled)
8. (Original) The dual mode built-in self-test controller of claim 6, wherein the memory built-in self-test signature includes a bit indicating whether a memory built-in self-test is done.
9. (Original) The dual mode built-in self-test controller of claim 1, wherein the memory built-in self-test engine comprises:  
a memory built-in self-test state machine; and  
a nested memory built-in self-test engine operating the memory built-in self-test state machine.
10. (Amended) The dual mode built-in self-test controller of claim 9, wherein the memory built-in self-test state machine ~~comprises~~ is configured to:  
enter a reset state ~~entered~~ upon receipt of an external reset signal;

enter an initiate state ~~entered from the reset state~~ upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

enter a flush state ~~entered from the initiate state~~ upon the initialization of components and signals in the memory built-in self-test domain in the initiate state;

enter a test state ~~entered into from the flush state~~ upon completing a flush of a plurality of memory components to a known state; and

enter a done state ~~entered into~~ upon completing the test of each of the memory components in the memory built-in self-test.

11. (Original) The dual mode built-in self-test controller of claim 1, wherein the memory built-in self-test engine comprises:

a plurality of alternative memory built-in self-test state machines; and

a nested memory built-in self-test engine operating a predetermined one of the memory built-in self-test state machines.

12. (Amended) The dual mode built-in self-test controller of claim 11, wherein each of the memory built-in self-test engines ~~comprises~~ is configured to:

enter a reset state ~~entered~~ upon receipt of an external reset signal;

enter an initiate state ~~entered from the reset state~~ upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

enter a flush state ~~entered from the initiate state~~ upon the initialization of components and signals in the memory built-in self-test domain in the initiate state;

enter a test state ~~entered into from the flush state~~ upon completing a flush of a plurality of memory components to a known state; and

enter a done state ~~entered into~~ upon completing the test of each of the memory components in the memory built-in self-test.

13. (Amended) A dual mode built-in self-test controller, comprising:
- a logic built-in self-test domain, including:
    - means for executing a logic built-in self-test; and
    - means for storing the results of a logic built-in self-test generated by an execution of the logic built-in self-test; and
  - a memory built-in self-test domain, including:
    - means for executing a memory built-in self-test;
- wherein the dual-mode built-in self-test controller is geographically centralized within an integrated circuit.
14. (Original) The dual mode built-in self-test controller of claim 13, wherein the logic executing means comprises:
- a logic built-in self-test state machine; and
  - a pattern generator capable of generating a scan pattern for use in a state of the logic built-in self-test state machine.
15. (Amended) The dual mode built-in self-test controller of claim 13, wherein the memory built-in self-test domain further comprises a means for storing the results of a memory ~~built-in~~ built-in self-test by an execution of the memory built-in self-test.
16. (Original) The dual mode built-in self-test controller of claim 13, wherein the memory executing means comprises:
- a memory built-in self-test state machine; and
  - a nested memory built-in self-test engine operating the memory built-in self-test state machine.
17. (Original) The dual mode built-in self-test controller of claim 13, wherein the memory executing means comprises:
- a plurality of alternative memory built-in self-test state machines; and
  - a nested memory built-in self-test engine operating a predetermined one of the memory built-in self-test state machines.

18. (Amended) An integrated circuit device, comprising:  
a plurality of memory components;  
a logic core;  
a testing interface; and  
a dual mode built-in self-test controller controlled through the testing interface,  
comprising:  
a logic built-in self-test domain, including:  
a logic built-in self-test engine capable of executing a logic built-in self-  
test on the logic core; and  
a logic built-in self-test signature generated by an execution of the logic  
built-in self-test; and  
a memory built-in self-test domain, including:  
a memory built-in self-test engine capable of executing a memory built-in  
self-test on the memory components;  
wherein the dual-mode built-in self-test controller is geographically  
centralized within the integrated circuit device.
19. (Original) The integrated circuit device of claim 18, wherein the logic built-in  
self-test engine comprises:  
a logic built-in self-test state machine; and  
a pattern generator capable of generating a scan pattern for use in a state of the  
logic built-in self-test state machine.
20. (Amended) The integrated circuit device of claim 18, wherein the memory built-  
in ~~self-test~~ self-test domain further comprises a memory built-in self-test signature  
register generated by an execution of the memory built-in self-test.
21. (Amended) The integrated circuit device of claim 18, wherein the memory built-  
in ~~self-test~~ self-test engine comprises:  
a memory built-in self-test state machine; and  
a nested memory built-in self-test engine operating the memory built-in self-test  
state machine.

22. (Original) The integrated circuit device of claim 18, wherein the memory built-in selftest engine comprises:  
a plurality of alternative memory built-in self-test state machines; and  
a nested memory built-in self-test engine operating a predetermined one of the memory built-in self-test state machines.
23. (Original) The integrated circuit device of claim 18, wherein the memory components include a static random access memory device.
24. (Original) The integrated circuit device of claim 18, wherein testing interface comprises a Joint Test Action Group tap controller.
25. (Amended) A method for performing a built-in self-test on an integrated circuit device, comprising:  
externally resetting a dual mode built-in self-test controller wherein the dual-mode built-in self-test controller is geographically centralized within the integrated circuit device;  
performing at least one of a logic built-in self-test and a memory built-in self-test from the dual mode built-in self-test controller; and  
obtaining the results of the performed built-in self-test.
26. (Original) The method of claim 25, wherein externally resetting the dual mode built-in self-test controller includes at least one of resetting a logic built-in self-test state machine in a logic built-in self-test engine and resetting a memory built-in self-test state machine in a memory built-in self-test engine.
27. (Original) The method of claim 25, wherein resetting the dual mode built-in self-test controller includes initializing a multiple input signature register and a pattern generator in a logic built-in self-test domain of the dual mode built-in self-test controller.
28. (Original) The method of claim 25, wherein performing the logic built-in self-test includes:

initiating a plurality of components and signals in a logic built-in self-test domain of the dual mode built-in self-test controller upon receipt of a logic built-in selftest run signal;  
scanning a scan chain upon the initialization of the components and the signals; stepping to a new scan chain; and  
repeating the previous scanning and stepping until the content of a pattern generator equals a predetermined vector count.

29. (Original) The method of claim 28, further comprising at least one of:  
setting a bit in the multiple input signature register indicating an error condition arose; and  
setting a bit in the multiple input signature register indicating whether the stored results are from a previous logic built-in self-test run.
30. (Original) The method of claim 25, wherein performing the memory built-in self-test includes:  
initiating a plurality of components and signals in a memory built-in self-test domain of the dual mode built-in self-test controller upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;  
flushing the contents of a plurality 'of memory' components to a known state after initialization of the components and the signals in the memory built-in self-test domain; and  
testing the flushed memory components.
31. (Amended) The method of claim 30, wherein performing the memory built-in self-test further includes at least one of:  
storing the results of the memory built-in self-test in a memory built-in self-test signature register; and  
~~storing the results of at least one paranoid check in the memory built-in self-test signature register;~~

setting a bit in the memory built-in self-test signature register indicating whether the memory built-in self-test is done.

32. (Amended) A method for testing an integrated circuit device, comprising:  
interfacing the integrated circuit device with a tester;  
externally resetting a dual mode built-in self-test controller wherein the dual-mode built-in self-test controller is geographically centralized within the integrated circuit device;  
performing a logic built-in self-test from the dual mode built-in self-test controller;  
performing a memory built-in self-test from the dual mode built-in self-test controller; obtaining the results of the performed logic built-in self-test and the performed memory built-in self-test.
33. (Original) The method of claim 32, wherein externally resetting the dual mode built-in self-test controller includes at least one of resetting a logic built-in self-test state machine in a logic built-in self-test engine and resetting a memory built-in self-test state machine in a memory built-in self-test engine.
34. (Original) The method of claim 32, wherein performing the logic built-in self-test includes:  
initiating a plurality of components and signals in a logic built-in self-test domain of the dual mode built-in self-test controller upon receipt of a logic built-in selftest run signal;  
scanning a scan chain upon the initialization of the components and the signals; stepping to a new scan chain; and  
repeating the previous scanning and stepping until the content of a pattern generator equals a predetermined vector count.
35. (Original) The method of claim 32, wherein performing the memory built-in self-test includes:  
initiating a plurality of components and signals in a memory built-in self-test domain of the dual mode built-in self-test controller upon receipt of at



least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

flushing the contents of a plurality of memory components to a known state after initialization of the components and the signals in the memory built-in self-test domain; and

testing the flushed memory components.

36. (Original) The method of claim 32, wherein obtaining the results includes reading at least one of a logic built-in self-test signature and a memory built-in self-test signature.
37. (Original) The method of claim 32, wherein interfacing the integrated circuit device with the tester includes employing Joint Test Action Group protocols.